Short Papers

A Low-Noise $K-Ka$ Band Oscillator Using AlGaAs/GaAs Heterojunction Bipolar Transistors

Mohammad Madihian and Hideki Takahashi

Abstract—**The design considerations, fabrication process, and performance of the first $K-Ka$ band oscillator implemented using a self-aligned AlGaAs/GaAs heterojunction bipolar transistor (HBT) are described. A large-signal time-domain based design approach has been used which applies a SPICE-F simulator to optimization of the oscillator circuit parameters for maximum output power. The oscillator employs a 2×10 μm^2 emitter AlGaAs/GaAs HBT fabricated using a pattern inversion technology. The HBT has a base current $1/f$ noise power density lower than 1×10^{-20} A^2/Hz at 1 kHz, and lower than 1×10^{-22} A^2/Hz at 100 kHz, for a collector current of 1 mA. The oscillator, which is composed of only low-Q microstrip transmission lines, has a phase noise of -80 dBc/Hz at 100 kHz off carrier when operated at 26.6 GHz. These results indicate the applicability of the HBT's to low-phase-noise monolithic oscillators at microwave and millimeter-wave frequencies, where both Si bipolar transistors and GaAs FET's are absent.**

I. Introduction

Stable local sources are required for microwave and millimeter-wave communication and measurement systems. Oscillators implemented with GaAs FET's can meet the frequency requirements, but they suffer from a high level of phase noise, which results from the baseband noisy characteristics of the device [1]. Oscillators fabricated with Si bipolar transistors, on the contrary, show excellent noise behavior, but they are available only up to about 20 GHz [2], and, moreover, monolithic integration of the entire circuit is impossible owing to the application of a conductive substrate.

III–V-based heterojunction bipolar transistors [3]–[6], on the other hand, are excellent candidates for low-phase-noise microwave and millimeter-wave monolithic oscillator applications, since they exhibit a low $1/f$ noise and respectable high-frequency performance. We have already reported on the 4 GHz and 15 GHz band hybrid IC (HIC) AlGaAs/GaAs HBT oscillators [7], [8]; these show a phase noise level of -65 dBc/Hz at 10 kHz off carrier, which is about 20 dB lower than that for a GaAs FET oscillator operating in the same frequency band and with the same circuit topology. The present paper reports on the results of a $K-Ka$ band oscillator implemented using an AlGaAs/GaAs HBT.

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II. Oscillator Circuit Design

A time-domain-based design tool has been applied for determining the circuit parameters of the AlGaAs/GaAs HBT oscillator. The approach uses the SPICE-F simulator with the device parameters modeled applying both measured dc characteristics and small-signal S parameters of a previously fabricated discrete HBT. Details of the algorithm utilized for determination of the HBT equivalent circuit parameters are described elsewhere [5].

The time-domain design approach is capable of predicting outpout power, efficiency, oscillation frequency, oscillation buildup characteristics, and bias voltage dependences—information that is indispensable for voltage-controlled oscillator (VCO) design in a phase locked loop (PLL) system—all in a single step. The approach is a large-signal design method, since the analysis is performed in the time domain taking into account the nonlinearity of the device elements and electrical characteristics. The time- and voltage-dependent nonlinear collector and base currents used in the simulation, which were proposed by Gummel and Poon [9], are given by

$$\begin{aligned} I_c(t,v) = {} & (I_{ES}/Q_B)[\exp(qv_{BE}/n_F kT)-1] \\ & -(I_{CS}/Q_B)[\exp(qv_{BC}/n_R kT)-1] \\ & -(I_{CS}/B_R)[\exp(qv_{BC}/n_R kT)-1] \\ & -J_{LC}[\exp(qv_{BC}/n_R kT)-1] \end{aligned} \quad (1)$$

and

$$\begin{aligned} I_B(t,v) = {} & (I_{ES}/Q_B)[\exp(qv_{BE}/n_F kT)-1] \\ & -J_{LE}[\exp(qv_{BE}/n_{LC} kT)-1] \\ & +(I_{CS}/B_R)[\exp(qv_{BC}/n_R kT)-1] \\ & -J_{LC}[\exp(qv_{BC}/n_{LC} kT)-1] \end{aligned} \quad (2)$$

where Q_B is the base charge, I_{ES} and I_{CS} are the base–emitter and base–collector junction leak currents, n_F and n_R are the base–emitter and base–collector junction ideality factors, n_{LE} and n_{LC} are the base–emitter and base–collector junction leakage ideality factors, and $v_{BE}=V_{BE}+v_{be}\sin\omega t$ and $v_{BC}=V_{BC}+v_{bc}\sin(\omega t+\phi)$ are the instantaneous base–emitter and base–collector voltages, respectively. The time- and voltage-dependent nonlinear base–emitter and base–collector capacitances, C_{BE} and C_{BC}, on the other hand, are modeled in the simulation by the sum of the diffusion and depletion layer capacitances and are given by

$$\begin{aligned} C_{BE}(t,v) = {} & \tau_F(qI_s/n_F kT)\exp(qv_{BE}/n_F kT) \\ & + C_{JE0}(1-v_{BE}/V_E)^{-Me} \end{aligned} \quad (3)$$

and

$$\begin{aligned} C_{BC}(t,v) = {} & \tau_R(qI_s/n_R kT)\exp(qv_{BC}/n_R kT) \\ & + C_{JC0}(1-v_{BC}/V_C)^{-Me} \end{aligned} \quad (4)$$

where τ_F and τ_R are the forward and reverse transit times, C_{JE0} and C_{JC0} are the zero-biased base–emitter and base–collector

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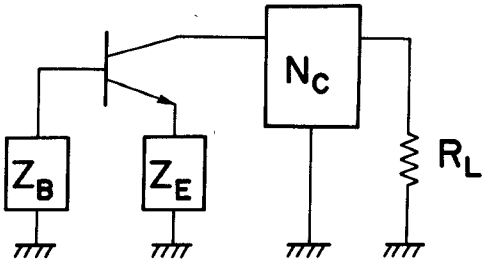

Fig. 1. A schematic diagram for a series feedback HBT oscillator.

TABLE I
SPICE-F PARAMETERS FOR AlGaAs/GaAs HBT

Emitter Size	2 μm×10 μm
RB	30 Ω
RE	9 Ω
RC	10 Ω
τF	2.5 ps
CJEO	37.5 fF
CJCO	30 fF

junction depletion layer capacitances, V_E and V_C are the base–emitter and base–collector built-in potentials, and *Me* and *Mc* are junction doping profile dependent numbers, ranging from 0.3 to 0.5.

A schematic diagram for the HBT oscillator is shown in Fig. 1. The oscillator uses a series feedback topology to facilitate integrability over a shunt feedback configuration, because the latter requires crossover of dc and RF circuits. In the figure, Z_B and Z_E are impedances responsible for providing a negative resistance at the HBT's collector terminal over a specific frequency band. N_C, on the other hand, is a matching network for satisfying the oscillation condition under maximum output power. Applying the SPICE-F model parameters for a 2×10 μm^2 AlGaAs/GaAs HBT, shown in Table I, Z_B, Z_E, and N_C were optimized for maximum output power at an oscillation frequency of 20 GHz. Here, Z_B and Z_E have been simulated by inductance L_B and capacitance C_E, respectively. N_C, on the other hand, has been expressed by a T network consisting of inductances L_1 and L_2 and capacitance C_1. $L_B = 1.4$ nH, $C_E =$ 40 fF, $L_1 = 1.5$ nH, $L_2 = 0.9$ nH, and $C_1 = 80$ fF are the optimum embedding circuit parameters estimated by the SPICE-F for a 20 GHz AlGaAs/GaAs HBT oscillator operating under maximum output power.

For a constant collector–emitter voltage, $V_{CE} = 3.7$ V, the oscillation buildup time is expected to increase with an increase in base–emitter voltage, V_{BE}, owing to an increase in base–emitter diffusion capacitance and, thus, in the positive feedback loop's charging time. This sets an upper limit on the applicable range of the base–emitter voltage, which is usually used as a control voltage of a VCO in a PLL system. On the other hand, for a constant base–emitter voltage, the output power first increases with collector–emitter voltage, but after reaching a peak it decreases as a consequence of the clipping characteristics of the device.

The flexibility of the oscillator circuit for operation at different frequency bands, by readjusting only Z_E, was investigated by changing C_E alone and simulating the oscillation frequency as well as the output power. Simulation results indicate that the circuit has the potential to oscillate at any single frequency in the 20–28 GHz band when C_E is changed in the 40–20 fF range.

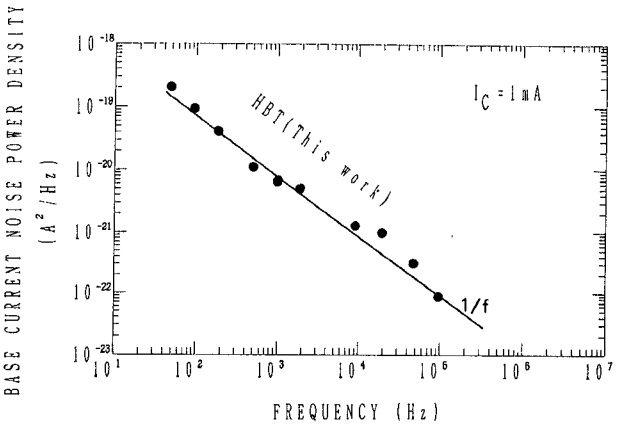

Fig. 2. Baseband noise characteristics for the 2×10 μm^2 HBT.

III. Fabrication Process and Device Performance

AlGaAs/GaAs epitaxial layer was used for the fabrication of the HBT employed in the oscillator chip. The structure consists mainly of a 0.15 μm $n = 3\times10^{17}$/cm^3 $Al_{0.25}Ga_{0.75}As$ emitter, a 0.1 μm $p = 3\times10^{19}$/cm^3 GaAs base, and a 0.5 μm $n = 5\times 10^{16}$/cm^3 GaAs collector. The HBT was fabricated in a self-alignment manner as explained here. After forming an SiO_2 dummy emitter, a closely spaced electrode process technology was employed to form the base contacts. Then, a pattern inversion method [10], [11] was used to expose the emitter layer for forming the emitter contact. Finally, after deposition of a CVD SiO_2 film on the wafer, this film, the base contact metal, and the base layer beneath it were selectively dry-etched, down to the collector layer, to form the collector contacts.

In this structure, a base surface recombination area, which is responsible for the $1/f$ noise generation and is defined by the undercut of the emitter mesa, is kept as small as 0.25×10 μm^2 in the case of a 2×10 μm^2 HBT. A proton ion-implantation technique was used for the device isolation and extrinsic base–collector capacitance reduction. AuMn and AuGe–Ni were used for the p-type and n-type ohmic contacts, respectively. The MMIC's bonding pads and transmission lines were Ti-Pt-Au and Au plated.

Fabricated 2×10 μm^2 HBT's exhibit a typical common-emitter current gain $h_{FE} = 30$, a transconductance $g_m = 80$ mS, and a collector–emitter breakdown voltage $V_{CEB} = 13$ V. Measured small-signal S parameters for a device over the 0.1–26.5 GHz frequency range resulted in an extrapolated short circuit current gain cutoff frequency of $f_T = 54$ GHz, and maximum oscillation frequency of $f_{max} = 45$ GHz.

To investigate the fabricated device's low-frequency noise characteristics, collector current noise power spectra for a 2×10 μm^2 HBT were measured using an HP3585A baseband spectrum analyzer and applied to calculate the base current noise power spectra. To facilitate observation of the $1/f$ noise component, a 1 kΩ feedback resistor was inserted between the emitter terminal and ground for reducing thermal noise power due to the base resistance at the collector terminal. Moreover, a 10 Ω load resistor was used at the collector terminal for amplifying the input noise to be observable by the measuring instrument. Results for a collector current $I_c = 1$ mA are represented in Fig. 2. The fabricated device has base current noise power densities of 1.0×10^{-20} A^2/Hz, 1.0×10^{-22} A^2/Hz, and 5×10^{-23} A^2/Hz, respectively, at 1 kHz, 100 kHz, and 200 kHz.

IV. Oscillator Performance

A chip photograph for the oscillator is shown in Fig. 3. The chip size is 1 mm×0.45 mm×0.15 mm. Recalling the figure, L_B

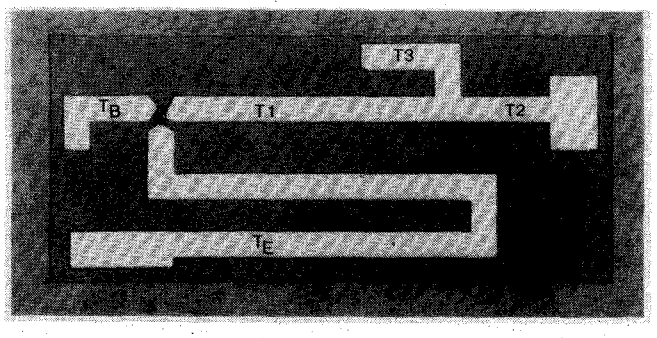

Fig. 3. Chip photograph for the 20–28 GHz AlGaAs GaAs HBT oscillator.

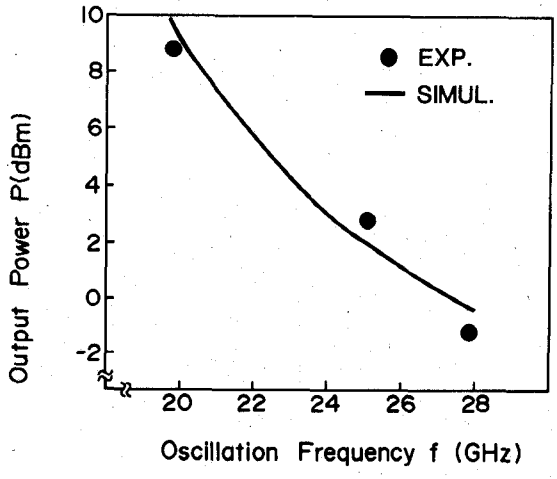

Fig. 4. Experimental and simulated power–frequency characteristics for the 20–28 GHz oscillator.

and C_E are, respectively, realized using short-circuited microstrip transmission lines T_B ($Z_0 = 70\ \Omega$, $l_B = 0.04\lambda$) and T_E($Z_0 = 70\ \Omega$, $l_E = 0.3\lambda$). On the other hand, L_1 and L_2 are formed using microstrip transmission lines T_1 ($Z_0 = 70\ \Omega$, $l_1 = 0.093\lambda$) and T_2 ($Z_0 = 70\ \Omega$, $l_2 = 0.037\lambda$), respectively, and C_1 is realized utilizing open-circuited microstrip transmission line T_3 ($Z_0 = 70\Omega$, $l_3 = 0.048\lambda$). In the above expressions, Z_0, λ, and l are, respectively, the characteristic impedance, the wavelength, and the electrical length of each line at 20 GHz.

Oscillator performance versus variation in both collector–emitter voltage, V_{CE}, and base–emitter voltage, V_{BE}, were investigated. Oscillation started at a collector–emitter voltage around 2.6 V and output power, P, was able to reach 9 dBm at oscillation frequency $f = 20.9$ GHz with a dc–RF efficiency of 19% for $V_{CE} = 5.2$ V and $I_c = 8$ mA. On the other hand, the oscillator's pushing figure was 900 MHz/V. Considering the theoretical results concerning the flexibility of the oscillator for operation at higher frequency bands, the effective length of transmission line T_E and, thus, the distributed capacitance C_E were changed by positioning the ground bond wires at different points along T_E. The oscillator could be operated at a frequency as high as 28 GHz for $l_E = 0.35$ mm, corresponding to $C_E = 20$ fF. The oscillator's power–frequency characteristics are shown in Fig. 4.

A free-running spectrum of the oscillator at a center frequency of 26.6 GHz for a span of 2 MHz and a resolution bandwidth of 10 kHz is shown in Fig. 5. Resultant phase noise is about -80 dBc/Hz at 100 kHz off carrier. Fig. 6 summarizes the phase noise behavior of previously reported GaAs MESFET and AlGaAs/GaAs HBT oscillators, including the present one,

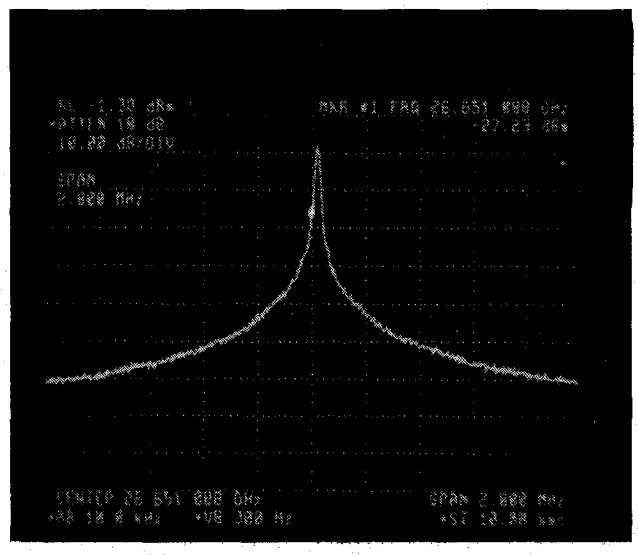

Fig. 5. A free-running spectrum of the oscillator at a center frequency of 26.6 GHz for a span of 2 MHz and a resolution bandwidth of 10 kHz.

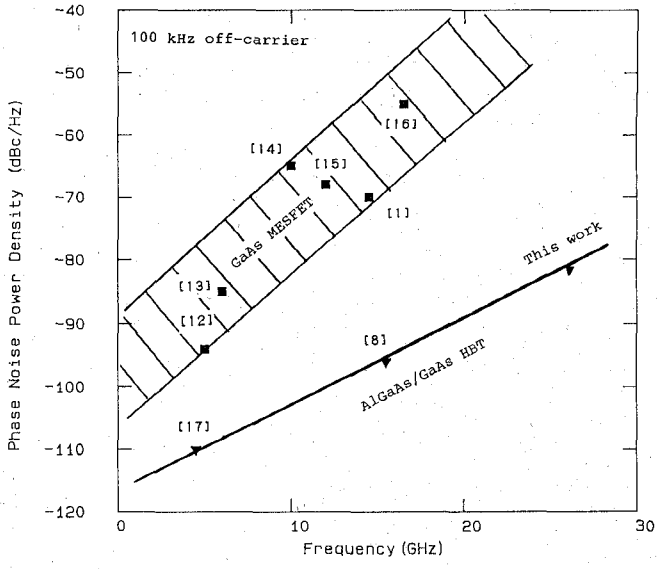

Fig. 6. Phase noise characteristics for GaAs MESFET and AlGaAs/GaAs HBT oscillators over a frequency range of 4 to 28 GHz at 100 kHz off carrier.

at 100 kHz off carrier, over a frequency range of 4 to 28 GHz [1], [8], [12]–[17]. The oscillators which apply a microstrip line structure have a low loaded Q of about 10 to 20. Extrapolating the results, the phase noise of the HBT oscillators is expected to be about 20 to 30 dB lower than that of the MESFET oscillators. Presuming that the oscillator phase noise is an up-conversion of the device's low-frequency noise into the carrier frequency, the HBT's are expected to have a $1/f$ noise about 20 to 30 dB lower than that of the MESFET's.

V. Conclusions

The design considerations, fabrication process, and performance of a K–Ka band oscillator implemented using a self-aligned AlGaAs/GaAs heterojunction bipolar transistor (HBT) have been described. A large-signal time-domain based design approach was applied to optimize the oscillator circuit parame-

ters for maximum output power. The oscillator uses a 2×10 μm^2 emitter AlGaAs/GaAs HBT fabricated by means of a pattern inversion technology. The HBT has a base current $1/f$ noise power density lower than 1×10^{-20} A^2/Hz at 1 kHz, and lower than 1×10^{-22} A^2/Hz at 100 kHz, for a collector current of 1 mA. The monolithic oscillator which operates over 20–28 GHz band has a phase noise of -80 dBc/Hz at 100 kHz off carrier when operated at 26.6 GHz. These results indicate the applicability of the HBT's to low-phase-noise monolithic oscillators at microwave and millimeter wave frequencies, where both Si bipolar transistors and GaAs FET's are absent.

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References

[1] B. T. Debney and J. S. Joshi, "A theory of noise in GaAs FET microwave oscillators and its experimental verification," *IEEE Trans. Electron Devices*, vol. ED-30, p. 769, July 1983.

[2] C. C. Leung, C. P. Snapp, and V. Grande, "A 0.5 μm silicon bipolar transistor for low phase noise oscillator applications up to 20 GHz," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1985, p. 383.

[3] H. Kroemer, "Heterostructure bipolar transistor and integrated circuits," *Proc. IEEE*, vol. 70, p. 13, Jan. 1982.

[4] N. Hayama, A. Okamoto, M. Madihian, and K. Honjo, "Submicrometer fully self-aligned AlGaAs/GaAs heterojunction bipolar transistor," *IEEE Electron Device Lett.*, vol. EDL-8, p. 246, May 1987.

[5] M. Madihian, K. Honjo, H. Toyoshima, and S. Kumashiro, "The design, fabrication, and characterization of a novel electrode structure self-aligned HBT with a cutoff frequency of 45 GHz," *IEEE Trans. Electron Devices*, vol. ED-34, p. 1419, July 1987.

[6] P. M. Asbeck *et al.*, "Heterojunction bipolar transistors for microwave and millimeter-wave integrated circuits," *IEEE Trans. Electron Devices*, vol. ED-34, p. 2571, Dec. 1987.

[7] M. Madihian, N. Hayama, K. Honjo, and H. Toyoshima, "A microwave AlGaAs/GaAs HBT oscillator," in *National Convention of IECE of Japan Dig.*, Mar. 1986, p. 253.

[8] N. Hayama, S. R. LeSage, M. Madihian, and K. Honjo, "A low-noise *Ku*-band AlGaAs/GaAs HBT oscillator," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 1988, p. 679.

[9] D. Warren, J. M. Golio, and E. Johnson, "Simulation of optically injection-locked microwave oscillators using a novel SPICE model," *IEEE Trans. Microwave Theory Tech.*, vol. 36, p. 1535, Nov. 1988.

[10] S. Tanaka, M. Madihian, H. Toyoshima, N. Hayama, and K. Honjo, "Novel process for emitter–base–collector self-aligned heterojunction bipolar transistor using a pattern-inversion method," *Electron. Lett.*, vol. 23, p. 562, May 21, 1987.

[11] M. Madihian, H. Shimawaki, and K. Honjo, "A 20–28 GHz AlGaAs/GaAs HBT monolithic oscillator," in *IEEE GaAs IC Symp. Dig.*, 1988, p. 113.

[12] C. Cu, H. Rohdin, and C. Stolte, "$1/f$ noise in GaAs MESFETs," in *IEEE IEDM Dig.*, 1983, p. 601.

[13] J. Sone and Y. Takayama, "A 7 GHz common drain GaAs FET oscillator stabilized with a dielectric resonator," *IECE of Japan, Monthly Meeting Report*, vol. MW-77, p. 59, 1977.

[14] G. Pataut and D. Pavlidis, "*X*-band varactor tund monolithic GaAs FET oscillators," *Int. J. Electron.*, vol. 64, p. 731, 1988.

[15] P. C. Wade, "*X*-band reverse channel GaAs FET power VCO," *Microwave J.*, p. 92, Apr. 1978.

[16] F. N. Sechi and J. E. Brown, "*Ku*-band FET oscillator," in *IEEE ISSCC Dig.*, 1980, p. 124.

[17] M. E. Kim *et al.*, "12–40 GHz low harmonic distortion and phase noise performance of GaAs heterojunction bipolar transistors," presented at the 1988 IEEE GaAs IC Symp., Nashville, TN, 1988.

Noise Power Sensitivities and Noise Figure Minimization of Two-Ports with Any Internal Topology

Janusz A. Dobrowolski

***Abstract*—A theoretical foundation is presented for the efficient CAD-oriented computation of first-order noise power sensitivities of networks with respect to network parameters. Application to the CAD of low-noise circuits with minimum noise figure using efficient gradient optimization methods is envisaged. The approach is applicable to circuits with any internal topology composed of any number of passive linear multiports and active linear two-ports. It is based on the scattering matrix description for circuit elements and wave representation for noise.**

I. Introduction

A recent paper by the author [1] presented a CAD-oriented noise analysis method for linear two-ports with absolutely general internal topology. The method allows noise figure computation of circuits which are composed of any number of passive linear multiports and active linear two-port devices.

The purpose of this paper is to present a computer-aided method for noise power sensitivity analysis of circuits of any topology. The noise power sensitivities are applicable to noise figure minimization of two-ports with any internal topology using gradient optimization methods. A scattering matrix and a wave representation are used for circuit and noise descriptions [2]–[4]. The approach may be used for noise performance optimization of such circuits as distributed amplifiers and amplifiers with any topology of feedback.

II. Noise Analysis

For a kth noisy element of a general circuit we can write the equation [1], [2]

$$\boldsymbol{B}^{(k)} = \boldsymbol{S}^{(k)}\boldsymbol{A}^{(k)} + \boldsymbol{B}_N^{(k)} \tag{1}$$

where $\boldsymbol{S}^{(k)}$ is the scattering matrix of the element, $\boldsymbol{A}^{(k)}$ and $\boldsymbol{B}^{(k)}$ are the vectors of ingoing and outgoing noise waves at its ports, and $\boldsymbol{B}_N^{(k)}$ is the vector of mutually correlated noise wave sources which represent noise generated in the element.

For a circuit composed of m elements (multiports) connected together by their ports (Fig. 1), we can write the following set of equations [1]:

$$\boldsymbol{W}\boldsymbol{A} = \boldsymbol{B}_N \tag{2}$$

where

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{A}^{(1)} \\ \boldsymbol{A}^{(2)} \\ \vdots \\ \boldsymbol{A}^{(m)} \end{bmatrix} \qquad \boldsymbol{B}_N = \begin{bmatrix} \boldsymbol{B}_N^{(1)} \\ \boldsymbol{B}_N^{(2)} \\ \vdots \\ \boldsymbol{B}_N^{(m)} \end{bmatrix} \tag{3}$$

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